Cipher-520
Hardware Reference Manual

V1.01

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1. Preface

This manual provides in-depth hardware informations of the Cipher-520 programmable terminal and serves as a reference for hardware and maintenance engineers. Assumption has been made that readers of this manual have basic knowledge of electric and/or electronic theory.

Numberings of all components, including connectors, passive and active components conform to the PCB V0.03. However, Syntech does not guarantee this conformity. The numberings and locations of components might be re-arranged. For confirmation, please refer to the PCB and its schematics. After all, this manual intends to describe the operation theory of the circuitry utilized.

2. General Features

The Cipher-520 is equipped with the followings,

- TLCS-900 16 bit CPU running at 14.7456 MHz
- Program : 512 KB flash memory
- Data memory : 128 KB battery back-up SRAM
- Memory card : optional, 512 KB to 2 MB SRAM (on a 512 KB basis)
- Fine-tunable calendar chip
- Memory & calendar chip backup 3.6V NiCd battery
- optional 1.2V X 7, 1200 or 1800 mAh rechargeable NiMH battery X 1 or 2 for operation backup
- Battery/external DC voltage monitor circuit on-board
- Self-shutdown circuit on-board (to prevent battery over-discharge)
- optional slot bar code reader or magnetic card reader
- 2 reader ports each for barcode scanners (Wand or Laser-emulation), or single/dual-track magnetic card readers
- 128X64 or 240X64 graphic type LCD display with LED back-light
- rubber keyboard (up to 8 X 8)
- up to 16 LEDs on the keyboard board
- 8 digital input/output, each can be configured to input or output
- external keyboard port for external PC/AT keyboard attachment
- RS232 port X 1
- Communication port X 2, each can be configured as CMOS RS232, RS232, RS485 (half-duplex), RS485 (full-duplex) or 20-mA current loop.

3. What's New

Compared to Cipher-510, many features have been enhanced and are listed below,

Item	510	520
CPU	16-bit CMOS CPU	same
CPU clock rate	9.8304	14.7456
LCD display	20X2	128X64 or 240X64
Battery	NiCd X 1	NiMH X 2
Keyboard	4 X 4 membrane	up to 8 X 8 rubber
Indicator	Good Read & Ready	also, up to 16 LEDs on the keyboard board
Program memory	128KB flash	512KB flash
Data Memory	up to 512 KB	up to 2MB + 128KB
Communication ports	fixed	configurable via add-on boards
Digital input/output	4/4	8, each configurable as input or output
power	1A switching regulator	2A, high efficiency switching regulator
fuse	none	resettable 1-Amp fuse X 2
speaker	yes	speaker or ear-phone
speaker volume	programmable	tunable via variable resistor

4. Characteristics

Basic characteristics of the Cipher-520 are listed below,

4.1. Electrical

- Main Power Supply Voltage : 12V ±5% DC
- Power consumption : 0.5W maximum with LCD backlight off and no external devices attached

4.2. Environmental

- Humidity (operating) : non-condensed 20% to 90%
- Humidity (storage) : non-condensed 10% to 95%
- Temperature (operating) : 0 to 50 °C
- Temperature (storage) : -20 to 70 °C
- EMC regulation : FCC class A and CE approved

4.3. Physical

- Dimensions : 261 X 125 X 100 mm (including battery holder)
- Weight : 1 Kg maximum including all batteries
- Material : ABS
- Color : dark-Gray

5. Nomenclature

5.1. Front view

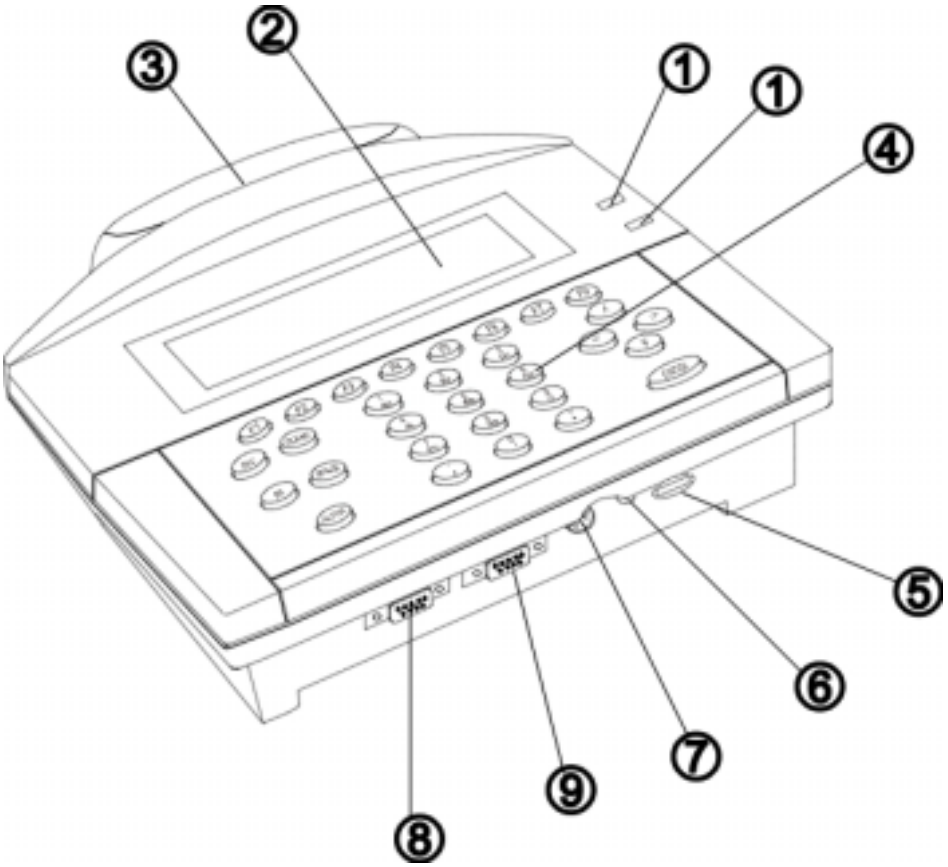


Figure 1 Front View

1) Red and Green LED for status indication
2) LCD display (240 X 64 or 128 X 64)
3) optional slot-type reader (barcode or magnetic card)
4) Keyboard
5) Volume
6) external ear-phone connector
7) external PC/AT keyboard connector
8) Reader port #1
9) Reader port #2

5.2. Rear View

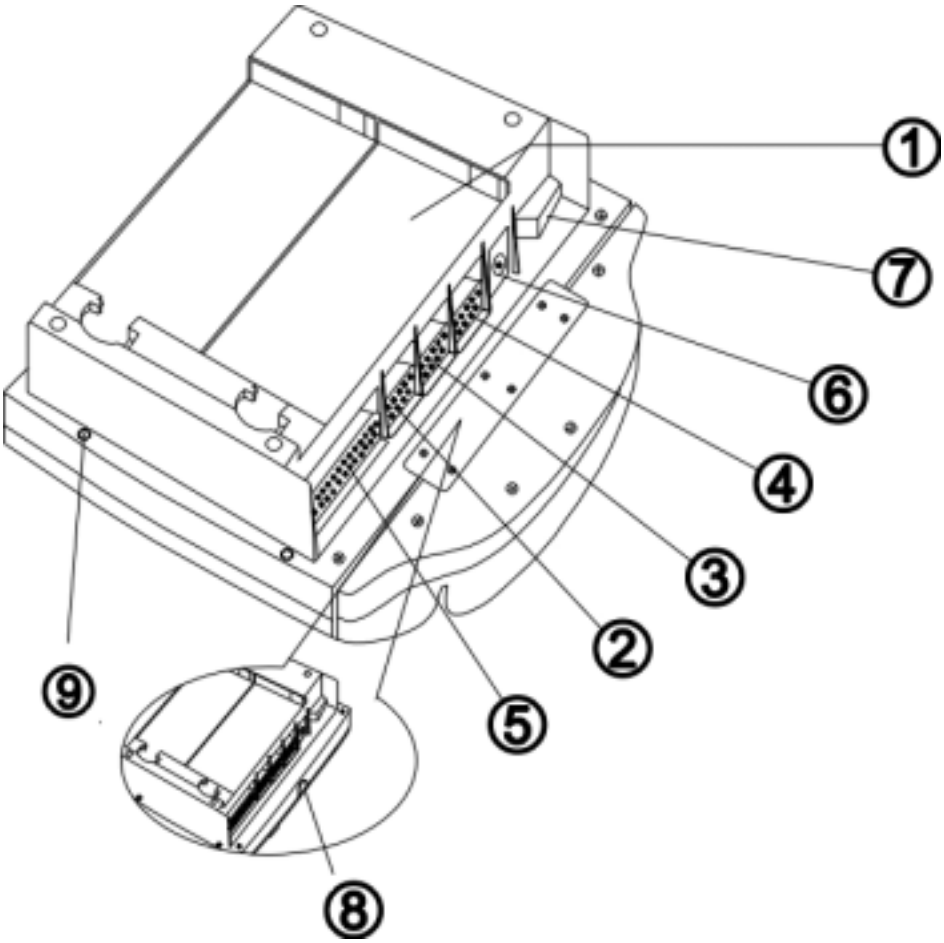


Figure 2 Rear View

1) Optional Operational Battery
2) COM1 connector
3) COM2 connector
4) COM3 connector
5) Digital input/output connector
6) external power DC-jack
7) Power switch
8) through-hole for slot reader cable
9) table stand mounting hole

6. PCB

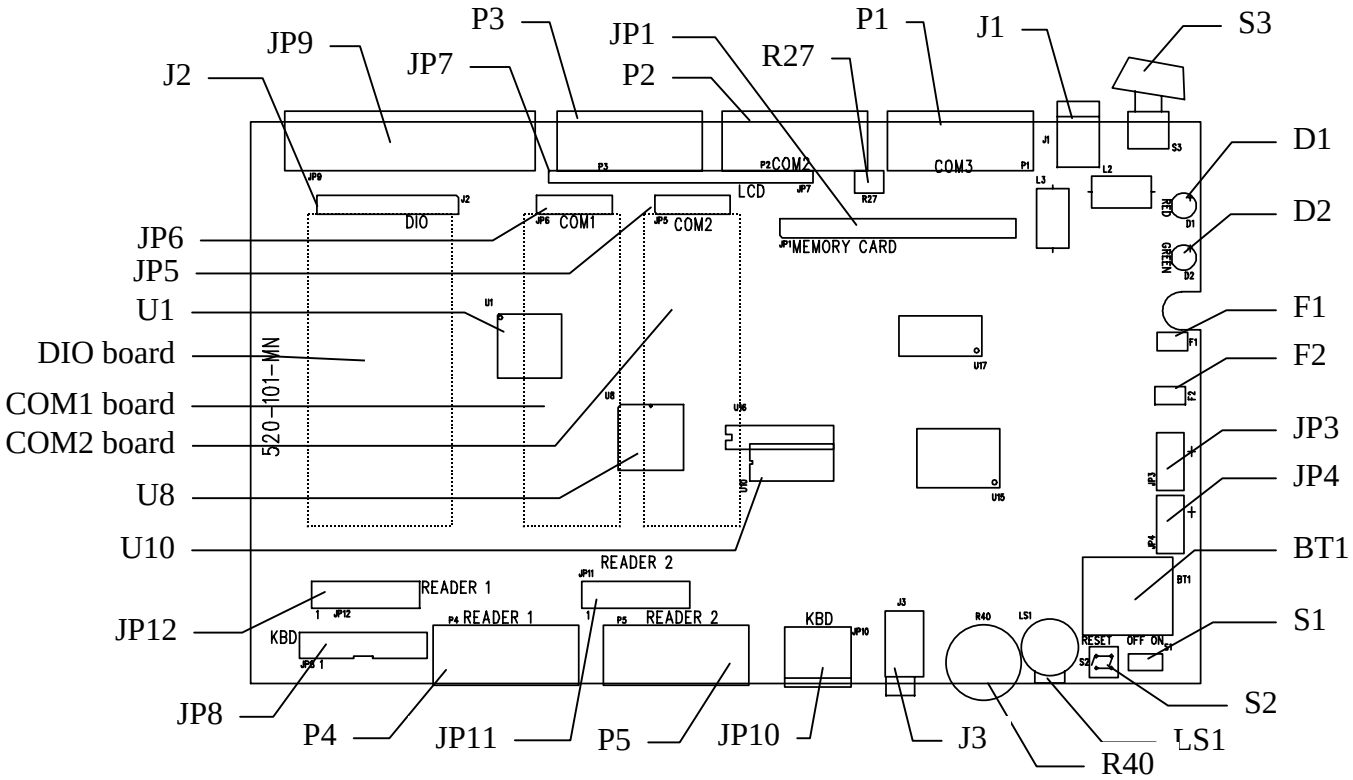


Figure 3 Main PCB front

1. JP9, digital I/O
2. P3, COM1
3. P2, COM2
4. P1, COM3
5. J1,+12V DC
6. S3,power switch
7. JP7, LCD connector
8. J2, DIO board connector
9. DIO board
10. JP6, COM1 board connector
11. COM1 board
12. JP5, COM2 board connector
13. COM2 board
14. R27, LCD view angle tuning
15. JP1, memory card connector
16. D1, red LED
17. D2, green LED
18. F1, 1-amp fuse for main board
19. F2, 1-amp fuse for external devices
20. JP3, battery #1
21. JP4, battery #2
22. JP8, keyboard connector
23. JP12, reader 1 connector
24. JP11, reader 2 connector
25. BT1, 3.6V NiHM battery
26. P4, reader 1
27. P5, reader 2
28. JP10, external AT keyboard
29. J3, ear-phone
30. R40, volume
31. LS1,Buzzer
32. S2, manual reset
33. S1, NiHM battery on/off
34. U1,CPU
35. U8,UART fot COM3
36. U10,calendar chip

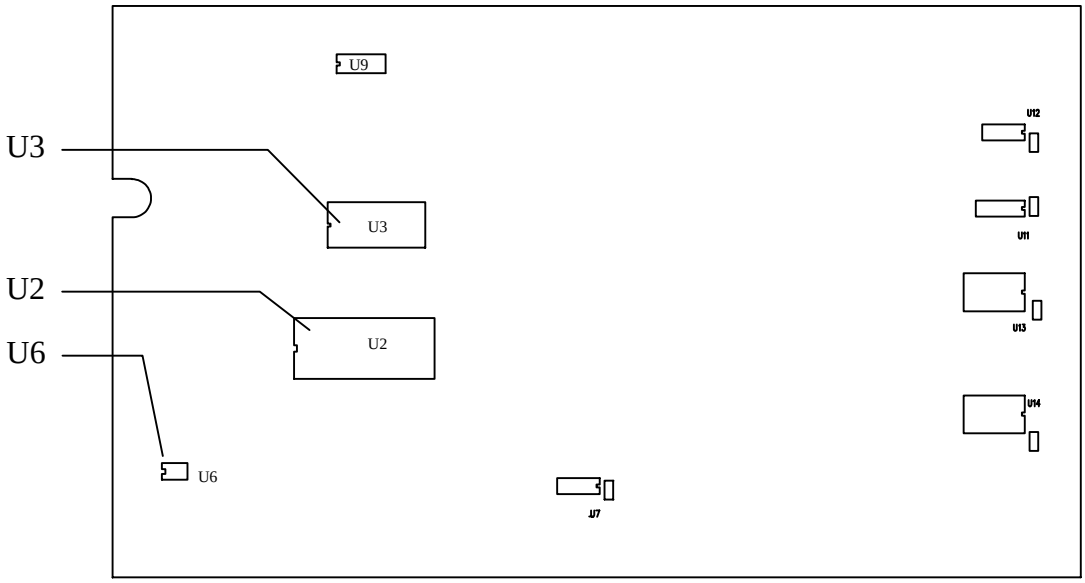


Figure 4 Main PCB back

1. U6,Reset
2. U3,1Mbit SRAM
3. U2,4 Mbit flash memory

7. Power Circuit

7.1. Power Source

The 520 can be powered from 2 sources : the external +12VDC or operation backup battery. If line power was down, the 1200 or 1800 mAh NiMH battery pack then took the place to provide the system power. The switching from external DC power to the battery is accomplished by a simple pair of diodes and is not even noticed by the operator.

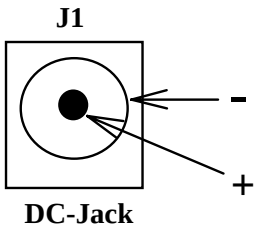


Figure 5 Main Power Connector

7.2. Switching Regulator

A high efficiency buck-type switching regulator (Maxim MAX1626) is used to generate the required system power (+5V). This regulator is capable of delivering up to 2 Amp current. And as a low on-resistance P-channel MOSFET has been used, the conversion efficiency is very high even at light loads (80% or more under 10 mA load. Low-ESR (equivalent series resistance) type tantalum capacitors are used both at input and output sides to reduce ripples.
Also, it is capable of 100% duty cycle operation. That is, when the input voltage is low (usually when the operational back-up battery is used and is almost drained), the MOSFET is turned on all the time. Thus, long working time utilizing the battery can be achieved.

7.3. Fuse

Two resettable fuses are used to protect the circuitry. These fuses are actually thermistor-like components whose resistance increase when temperature rises (results from large current flows through) and thus current flows through are limited. Since it is not actually broken as traditional fuses, replacement is not needed.

- F1 : main board, add-on boards (memory card, DIO card, COM cards and so on)
- F2 : external devices such as readers, PC/AT keyboards and so on.

8. Operation Battery

8.1.1. Battery

To facilitate procurement, off-the-shelf battery pack is used as follows,

- NiMH, 1.2V X 7, free of memory effect
- 1200 or 18000 mAh

After fully charged, if LCD backlight is on and no external devices been attached, one battery pack can last for 2.5 hours. Of course, if longer working time is required, both battery packs can be equipped to double it.

8.1.2. Charging

The charging current is typically 36 mA = 0.02C. In this way, the battery pack can be fully charged (from fully drained) in about 60 hours. This is also the safe charging current when the battery pack is fully charged. Else heat will be generated and shall damage or shorten useful life of the battery pack.
Note that this is not a software controllable charging. As long as the main power (+12V) is available, even if the power switch is off, this charging is taken in place.

8.1.3. Maintenance

Normally, the NiMH battery is guaranteed to work for 300 charge/discharge cycles while preserves at least 60% of its original capacity. However, it features a self-discharging characteristic even when it is disconnected. After a long-term storage (even when it is new), several charge/discharge cycles should be exercised to restore its specified capacity. On the shelf battery chargers can be used for this purpose.

8.1.4. Protection & Shutdown

The typical voltage for a NiMH battery cell is 1.2V and can be charged up to 1.4V or even 1.5V when fully charged. When the battery is fully charged, only a small amount of current can be asserted into the battery. As long as the charge current is within the specified trickle charge current limit (0.04 C), the battery will not be damaged. However, deep discharging the battery degrades its useful life or even cause permanent damage such as polarity reversal. A monitoring and shutdown circuitry is used to prevent this from happening. The battery voltage is feed to the CPU on-chip ADC via a resistor divider and then is checked by the program. If the battery was drained, the system will shutdown the system power.

During the discharging cycle (from fully charged to drained), the battery voltage drops rapidly at the beginning and then stays around 1.2V during most of the cycle (~70%). Finally when it is about to be drained, the voltage starts to drop again. Unfortunately the battery voltage alone is not sufficient to decide the remaining capacity of the battery. The recommended voltage level is 1.1V per cell for battery low and 1.0V for drained. That is, if the whole battery pack drops to below 6.0V, it is considered to be drained and the system power will be shutdown.

The shutdown is accomplished by a Flip-Flop and its glue circuits. Its output is reset to low (power enabled) during power on. A CPU output pin can then set it to high (to shutdown the switching regulator) by sending a negative going pulse. An R-C network prevents power-on spikes to false-trigger the circuit by disabling it for the starting 50ms. After shutdown, this Flip-Flop is still powered to keep this shutdown signal, which however consumes very little current. The shutdown signal stays even if the main power is asserted again. To restart the machine, the power switch must be turned off and then on again.

9. Reset

The system reset signal is generated by a voltage detector chip Maxim MAX703 (or compatible chips). It outputs an active low reset signal when the system power drops below a pre-determined voltage level (Vdet-). The reset signal then changes to high when the power is higher than another pre-determined voltage level (Vdet+). The Vdet+ is about 200 mV higher than Vdet-. This is known as hysteresis, and it prevents noise from false-triggering the reset circuitry. The TLCS-900 is guaranteed to work within 5V ±10%, and the Vdet- is set to 4.6V. This reset signal does not only ensure the proper operation of the CPU but also is used to reset the UART chip (NS82C50) and control SRAM access (connecting to SRAM CE2) during power-up and power-down. The later is very important as the SRAM contents might be changed by unwanted spikes during supply voltage changes.

Besides this basic function, this chip also provides power supply switching between +5V and back-up battery (for SRAM, calendar and so on). That is, when power switch is off, the SRAM contents can be preserved and the calendar chip running is not interrupted.

10.CPU

The CPU used in 520 is a Toshiba 16-bit CMOS CPU TMP95C061 and features the follows,

- Clock rate up to 20 MHz (14.7456 MHz for 520)
- mixed 8/16-bit data bus widths
- direct addressing up to 16 Mbytes
- 2 UART ports
- 4 8-bit timers
- 2 16-bit timers
- 10s of I/O ports depends on application
- 4 10-bit ADC channels

11. Program Memory (Flash)

4 MBit flash memory (AMD 29F400BT or the likes) is used to store the program code, font and so on and features the follows,

- guaranteed 100,000 erase/program cycles
- single +5V for read, erase and programming
- 11 blocks each can be individually erased and re-programmed
- 8/16 bits data bus

To facilitate program execution performance, this flash memory is accessed via a 16-bit data bus. A 150-ns or faster access time type flash is used to accommodate the CPU rate.

12. Flash writer

Normally, contents of the flash (e.g. application program) can be updated by using the 520 itself (of course, by proper programming). However, it is possible that the flash might get corrupted by improper usage or accident. Since the 520 then cannot even start-up properly. There must be some ways to re-program the flash memory. A flash writer card has been developed by Syntech to prevent nasty soldering. This card is able to program the flash memory when it is already on the 520 board. For detail usage and information of this card, please refer to its operation manual.

13. Data Memory (SRAM)

A 1 Mbit low power SRAM is equipped for program variables, data and so on. Its contents are backed up by the on-board 3.6V NiMH battery. A 150-ns or faster access time type SRAM is used to accommodate the CPU rate.

14.Calendar chip

A battery backup calendar chip is used to retain the system time even when power is off. The chip utilized is a V3022 from EM micro-electronic Marin SA. It features the following outstanding features,

- Very low power consumption
  When powered from the battery (3.6V), the current is typically 0.9μA.
- Wide operation voltage range
  This chip works down to 2V.
- On-chip high precision oscillator
  This is a must for accurate time keeping. The oscillator is built-in inside the chip and is factory trimmed.
- Timer Adjustment
  It can also be fine tuned to compensate for a fast or slow clock. This is an outstanding feature for those applications which need absolute accurate system time such as a time/clock application. The tuning of the calendar chip is done by modifying the value of the **trimming register** of the calendar chip.
- Trimming Register
  The speed of the calendar chip can be tuned in units of ppm via a digital trimming register. The trimming range is from 0 to 255 ppm. The bigger the value of the trimming register the slower the calendar chip runs. For instance, if the calendar chip is 1 second **slow** in one day then the value of the trimming register should **decrease** 12 to correctly adjust the calendar chip. During system initialization, this register is set to 186.

  1 sec/ 1 day = 1000000 / (24 hours * 60 min * 60 sec) = 11.57 ppm ~= 12 ppm
- Write-protected
  The time and trimming register are write-protected, and they won't be changed accidentally.
- Cold start detection
  There is a cold start bit in the chip. This bit is set if power loss encountered or on first power-on. The software can then recognize this bit and initialize the calendar chip.

15. Memory and Calendar Backup Battery

A 3.6V rechargeable NiMH battery is used to backup the SRAM and keeps the calendar chip running even when system power is off. Its capacity is 60 mAh and is trickle charged with a typical 1.2 mA current. After fully charged, it is able to sustain for more than 15 months as follows,

- SRAM (LL-type, SONY CXK581000)
  current consumed is 0.7μA (typical) and 4μA (max, 0 to 40°C)
- V3022 : 0.9μA (typical), 1.5μA (max.)

Time (typical) = 60 mAh / (0.7 + 0.9) = 37500 hrs = 1562 days > 52 months
Time (worst) = 60 mAh / (4.0 + 1.5) = 10909 hrs = 454 days > 15 months

A switch is equipped to disconnect and preserve battery power when the 520 is not to be used for a while (e.g. during shipping). This switch **must be normally turned on** else the SRAM contents and system time will get lost once the 520 was turned off. However, the 520 can still work properly regardless of this switch setting since the SRAM and calendar chip is at that time supplied by the system +5V.

16. LCD

Two types of LCD displays can be used in 520 as follows,

- 240 X 64 dots
- 128 X 64 dots

Both are STN type graphic display equipped with LED back-light.

The typical back-light current for 240X64 type is 320 mA.

JP7

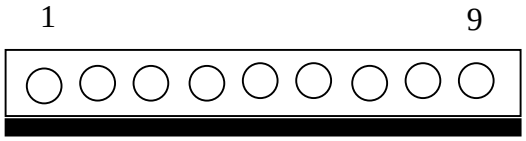
Figure 6 LCD Connector

This is a 22-pin SIP (single-in-line 2.54 mm pitch) connector.

1. Ground
2. Vcc, +5V
3. Vo, view angle control
4. A1 (address bus)
5. read/write control
6. chip enable
7. D8 (data bus)
8. D9 (data bus)
9. D10 (data bus)
10. D11 (data bus)
11. D12 (data bus)
12. D13 (data bus)
13. D14 (data bus)
14. D15 (data bus)
15. chip select #1
16. chip select #2
17. reset
18. Vee, -10V
19. LED backlight anode, shorts to +5V
20. LED backlight cathode
21. LED backlight anode, shorts to +5V
22. LED backlight cathode

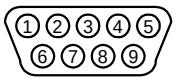
17.Reader

There are total 2 reader ports provided, each can be either a Barcode slot reader, Barcode Scanner (Wand/Laser emulation), or up to dual-track magnetic card reader. They are equivalent in both hardware and software. Their connectors and pin-assignments are listed below. Beware that, in order to decode barcode and magnetic card at the same time, some signals share the same pin. However, the software is able to tell which type of the readers are attached.



JP 11 & 12, male 2.54 mm SIP

DB-9 Male



Front Veiw

P4 & P5, D-type 9-pin male

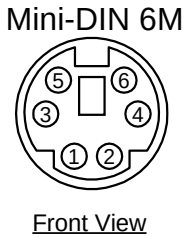
Figure 7 Reader Connector

JP11 & 12	Barcode	Magnetic	P4 & P5
1	Start Of Scan	Not used	1
2	Data	Clock 1	2
3	Good Read	Not used	3
4	Not Used	Data 1	4
5	Switch	Clock 2	5
6	Power Enable	Not used	6
7	Ground	Ground	7
8	Not used	Data 2	8
9	Vcc, +5V	Vcc, +5V	9

The JP11 and JP12 are mainly for attaching slot-type readers. And since they share the same signal lines as P4 and P5. They should not be used at the same time. For example, if JP11 is attached to the slot type MSR then P4 should not be used, else fault would occur.

18. External PC/AT Keyboard

Besides the built-in rubber keyboard, an external PC/AT keyboard can be attached for handy data entry. The connector and pin assignment conforms to PC/AT standard keyboard.



Front View

JP10, mini-DIN 6-pin, female

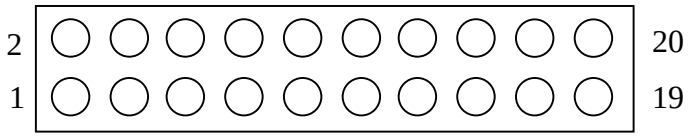
Figure 8 External Keyboard Connector

1. N.C.
2. data
3. +5V
4. Ground
5. N.C.
6. clock

19. Keyboard & indicators

An 8 by 8 scanning circuitry has been reserved for accessing the built-in rubber keyboard and LED (up to 16) indicators. The standard keyboard provides the following keys,

- numbers 0~9
- function keys, F1-F8 (each has an corresponding LED)
- ESC, escape
- clear
- BS, back space
- Space
- Alpha, toggle between numbers and alphas (with LED)
- 4 direction keys (up, down, right and left)
- Enter



JP8, 10 X 2 2.54 mm male connector

Figure 9 Keypad Connector

1. D8	11. D13
2. Vcc, +5V	12. Ground
3. D9	13. D14
4. Ground	14. Ground
5. D10	15. D15
6. out select	16. Vcc, +5V
7. D11	17. Keyboard ID0
8. in select	18. Keyboard ID1
9. D12	19. Keyboard ID2
10. LED enable	20. Keyboard ID3

20. Memory card

The data memory can be extended by adding an optional memory card. Which is able to provide 512 KByte to 2 Mbyte SRAM (on an 512 KB basis since 4 Mbit size SRAMs are used). Contents of these SRAMs are backed by an on-board 3.6V NiMH battery (same type of battery used on main board). 2 slide switches are used for,

- Battery on/off, if the memory card is not to be used for a while. This switch can be set to OFF to preserve battery power. Of course, under normal use, it MUST be set ON.
- Memory access on/off, when set to OFF, access to these SRAMs are denied. This is usually used when a memory card is to be switched from one terminal to another. However, care should be taken that the battery ON/OFF switch should be at the ON position else SRAM contents would be lost. Also, under normal use, it should be set ON.

Since the flash writer (which we have mentioned in prior section) uses the memory card connector also. A JP2 connector is intentionally left on the board such that the flash writer can still be used when the memory card is equipped.

Also, like the battery on the main board, the 3.6V NiHM battery is charged by the system +5V. After fully charged, the data retention time is estimated below,

SRAM (LL-type, SONY CXK581000)
current consumed is 0.7μA (typical) and 4μA (max, 0 to 40°C)

Time (1 SRAM, typical) = 60 mAh / (0.7) = 85714 hrs = 3571 days > 119 months
Time (1 SRAM, worst) = 60 mAh / (4.0) = 15000 hrs =625 days > 20 months

More SRAMs are equipped, less data retention time.

21. COM port

There are totally 3 serial communication ports, namely COM1, COM2 and COM3. They all features DB-9 female connector as depicted below,

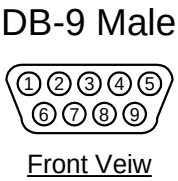


Figure 10 COM port Connector

For flexibility, for COM1 & 2, 4 kinds of COM boards can be attached to accommodate application needs as follows,

- RS232
- Half-duplex RS485
- Full duplex RS485
- 20 mA current loop

Whereas the COM3 has been fixed to RS232.

21.1.1. RS232

This is an EIA-RS232C compatible interface and provides 4 signals as follows,

No.	Description	No.	Description
1	Ground	6	No connection
2	Transmit data	7	CTS
3	Receive data	8	RTS
4	No conenction	9	+5V
5	ground		

21.1.2. Half-duplex RS485

This is a differential serial communication interface where all terminals send and receive data from a pair of signal lines.

No.	Description	No.	Description
1	Non-inverting data	6	No connection
2	Ground	7	No connection
3	Inverting data	8	No connection
4	No connection	9	+5V
5	No connection		

21.1.3. Full duplex RS485

This is a differential serial communication interface where all terminals send and receive data each from a pair of signal lines.

No.	Description	No.	Description
1	Non-inverting transmit data	6	ground
2	Ground	7	Inverting receive data
3	Inverting transmit data	8	No connection
4	No connection	9	+5V
5	Non-inverting receive data		

RS485 transceivers (both half and full duplex board) are protected by a pair of surge protectors. Also, when the terminal is at either end of the RS485 bus, a terminator should be used to cancel signal echoing. This can be easily done by putting the slide switch to ON position (move the switch to your right hand), which will connect 3 resistors onto the bus as follows,

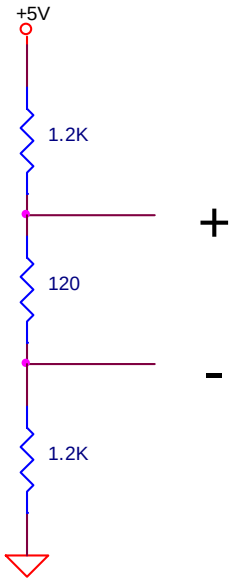


Figure 11 RS485 terminator

21.1.4. 20-mA current loop

This is usually used when electrical isolation between communication sides are required. Pin assignments of the 20-mA current loop are as follows,

No.	Description	No.	Description
1	Transmit power	6	Receive cathode
2	Transmit collector	7	Ground
3	Transmit emitter	8	Ground
4	Receive power	9	+5V
5	Receive Anode		

Both transmit and receive part can work in either active (providing power) or passive (getting power from external device) mode.

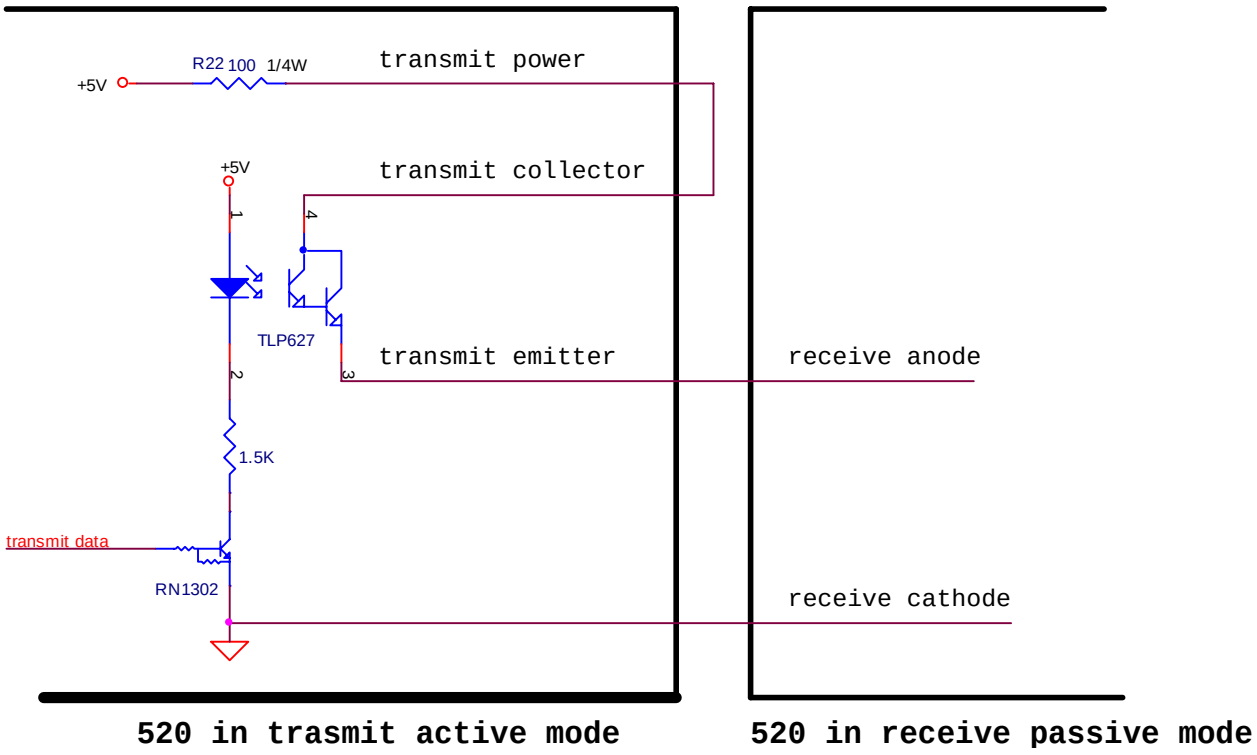


Figure 12 20 mA current loop transmit connection

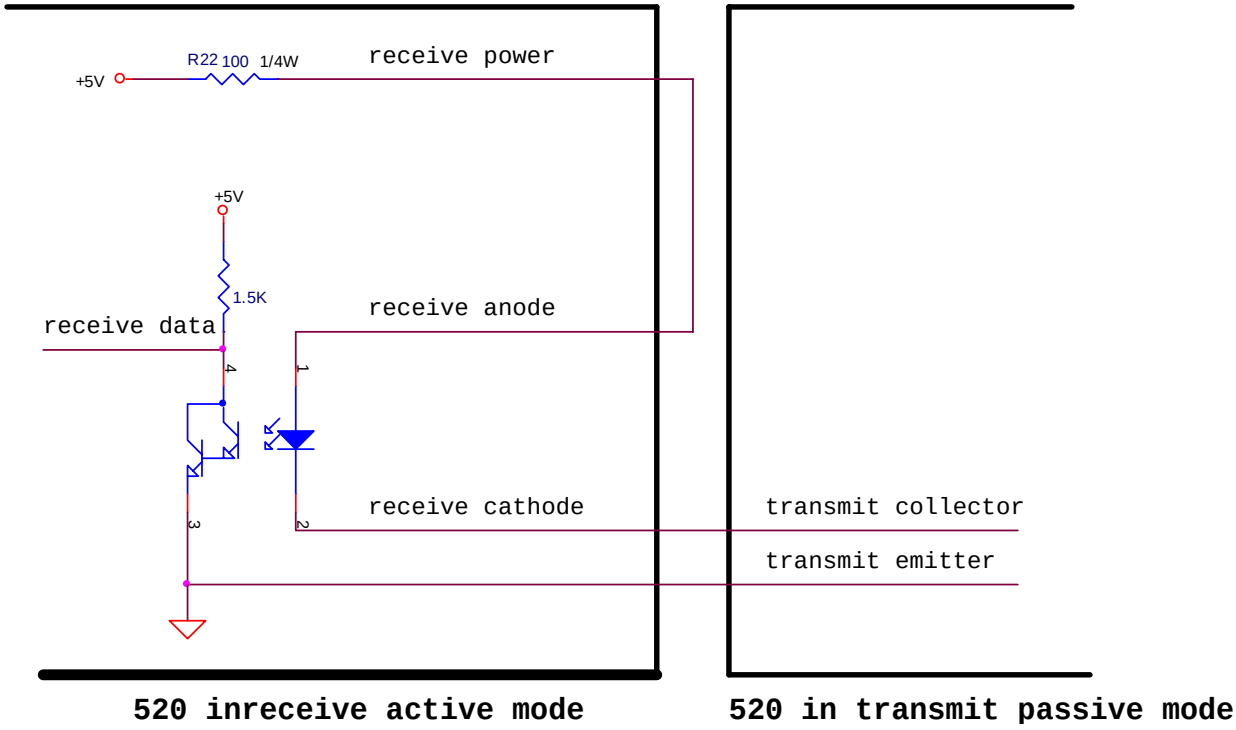
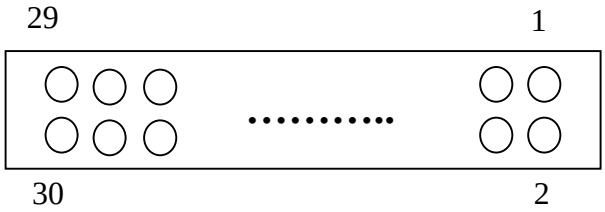


Figure 13 20 mA current loop receive connection

22. Digital Input / Output

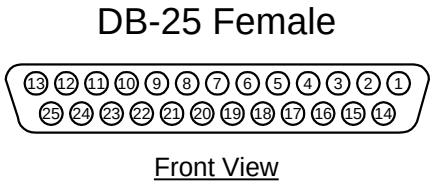
8 digital input/output pins has been reserved and each can be individually set to input or output. An optional DIO board can be used to accommodate kinds of input/output needs



J2, dual-in-line (15 X 2) 2.54 mm male connector

Figure 14 DIO board connector

No.	Description	No.	Description
1	Vcc, +5V	3-10	DIO #1~8
2	Ground	4-30	Shorts to JP9 pin 3 to 22



JP9, D-type 25 pin Female connector

Figure 15 DIO connector

No.	Description	No.	Description
1	Ground	23	+5V
2	Ground	24	+5V
3-22	DIO board dependent	25	+5V

22.1. Digital Input

2 kinds of digital inputs are available,

- CMOS type

This is the +5V CMOS type digital signal. For 4I/4O board, pin assignments of JP9 are as follows,

No.	Description
5	DI #1
7	DI #2
9	DI #3
11	DI #4

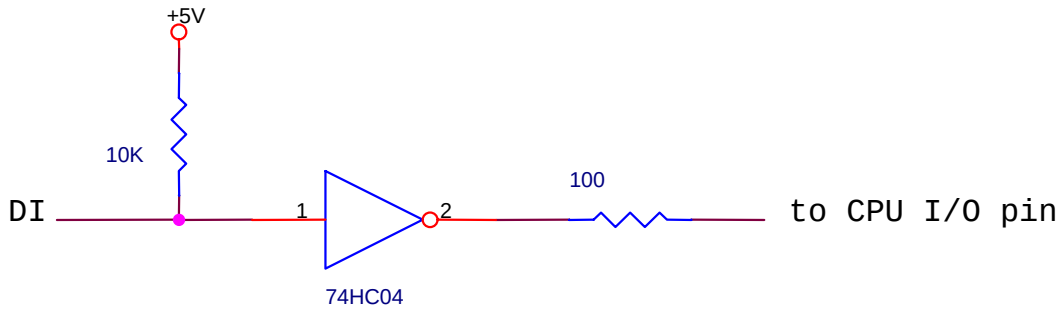


Figure 16 CMOS level DI

- Photo-coupled

  This is used when electrical isolation is required.

No.	Description
5	DI #1 anode
6	DI #1 cathode
7	DI #2 anode
8	DI #2 cathode
9	DI #3 anode
10	DI #3 cathode
11	DI #4 anode
12	DI #4 cathode

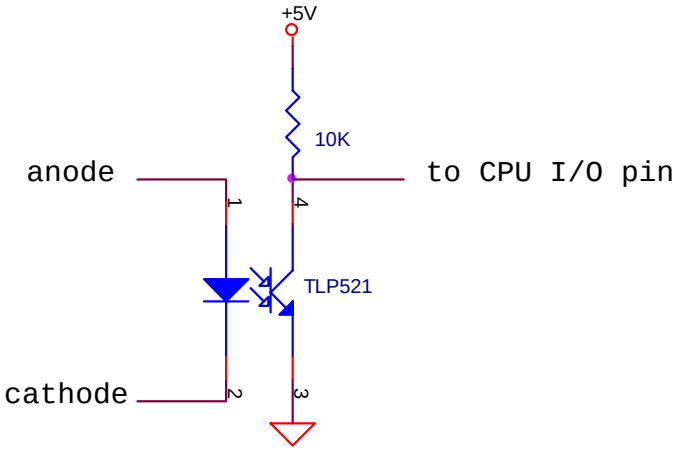


Figure 17 Photo-isolated DI

Characteristics of the TLP-521 are listed below,

1) LED
   - Maximum Forward current : 70 mA
   - Pulse forward current : 1 A
   - Maximum reverse voltage : 5V
   - Forward voltage (at 10 mA) : 1.15V (typical), 1.3V (maximum)
   - Reverse current : 10μ A (maximum)

2) Output Transistor
   - Collector-Emitter breakdown Voltage : 35 V
   - Emitter-Collector breakdown Voltage : 7 V
   - Maximum Power dissipation : 150 mW
   - Maximum collector current : 50 mA
   - Collector dark current (at 25°C) : 100 nA maximum
   - Collector dark current (at 85°C) : 50μA maximum
   - Current transfer ratio : 100%(minimum), 600% (maximum)
   - Isolation resistance : $10^{11}\Omega$ (typical)
   - Isolation Voltage : 2500 Vrms (typical)

The transistor collector is pulled up by Ri, a 10K resistor and then feed to CPU input pin, which features a low threshold of 0.8V and high threshold of 2.2V. That is, the collector voltage must be no more than *0.8V* to be treated as *low* and no lower than *2.2V* to be treated as *high*.

22.1.1. Input High

Ideally, when there is no current flowing through the input LED, the output transistor is off and the collector is pulled up to +5V. However, leakage current does exist. Assume a small leakage current flows through the LED then,

collector voltage Vc = +5V - (Ic * Ri) ≥ 2.2 V

where Ic is the collector current and = collector dark current + (LED leakage current * current transfer ratio)

The lowest collector voltage(worst case) = 5.0 - ((50μA +(IL * 600%) * 10 K)

5 V - 0.5 V - 60000 * IL ≥ 2.2 V and IL ≤ 38 μA

That is, the leakage current into the LED should not be larger than 38μA, however this is much higher than the LED leakage current 10 μA and false trigger is not likely to happen.

22.1.2. Input Low

To input a low, the external device must supply a large enough current to flow through the LED to turn on the transistor and pull collector no higher than 0.8V. This LED current can be calculated similar to the case for input high.

5V - 0.5V - (100% * IL * 10K) ≤ 0.8 V
then IL ≥ 0.37 mA

That is, to pull the digital points low, there must be at least 0.37 mA current flowing through the LED. For example, to connect an external dry contact to the digital inputs,

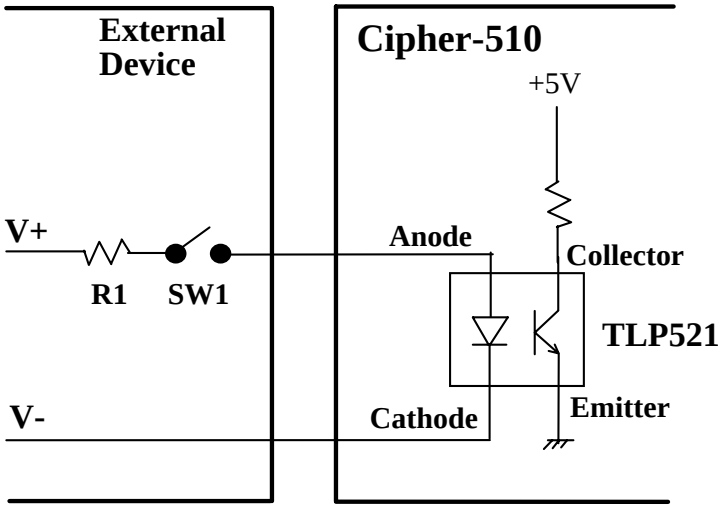


Figure 18 Digital Input Example

LED current IL = $(V_+ - V_- - V_f) / (R_1 + R_{on})$ 0.37 mA = 1 mA (safe margin)
Where V_+ : positive supply voltage of the external device
V_- : negative supply voltage of the external device
V_f : LED forward voltage
R_1 : current setting resistor
R_{on} : switch contact resistance

If $(V_+ - V_-) = 5V$ and maximum R_{on} is 10Ω then,
$(5 - 1.3) / (R_1 + 10) \geq 1$ mA, $R_1 \leq 3.7K\Omega$

22.2. Digital Output

3 kinds of digital outputs are available,

- CMOS level DO

For 4I/4O board, pin assignments of the JP9 are as follows,

No.	Description
13	DO #1
15	DO #2
17	DO #3
19	DO #4

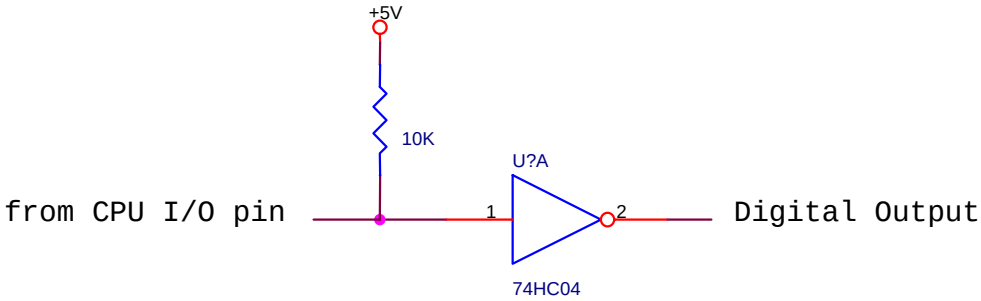


Figure 19. CMOS level DO

♦ Open-collector DO

For 4I/4O board, pin assignments of the JP9 are as follows,

No.	Description	No.	Description
3 & 4	Common	17	DO #3
13	DO #1	19	DO #4
15	DO #2		

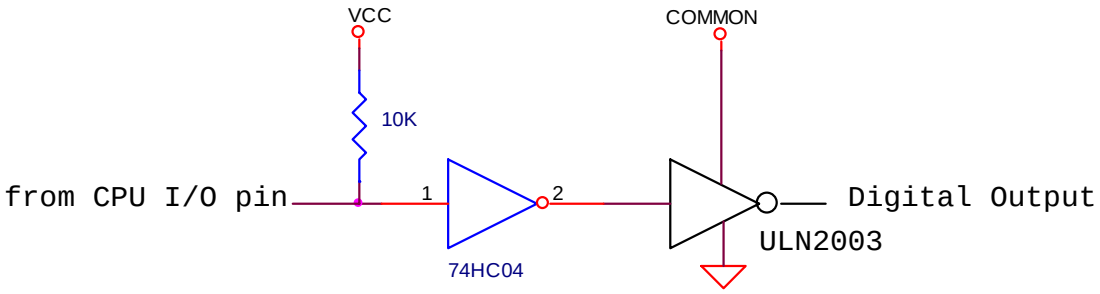
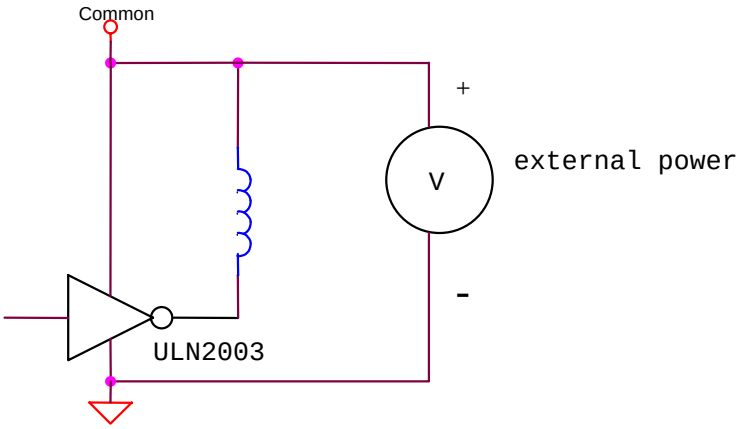


Figure 20. Open collector DO

Care should be taken that if inductive type load is to be connected, the COMMON point can be used for inductor inherent reverse EMF suppression. For example,



This would connect the ULN2003 internal suppressing diode across this inductive load.

♦ Relay Output

For 4I/4O board, pin assignments of the JP9 are as follows,

No.	Description	No.	Description
13	DO #1, contact #1	17	DO #3, contact #1
14	DO #1, contact #2	18	DO #3, contact #2
15	DO #2, contact #1	19	DO #4, contact #1
16	DO #2, contact #2	20	DO #4, contact #2

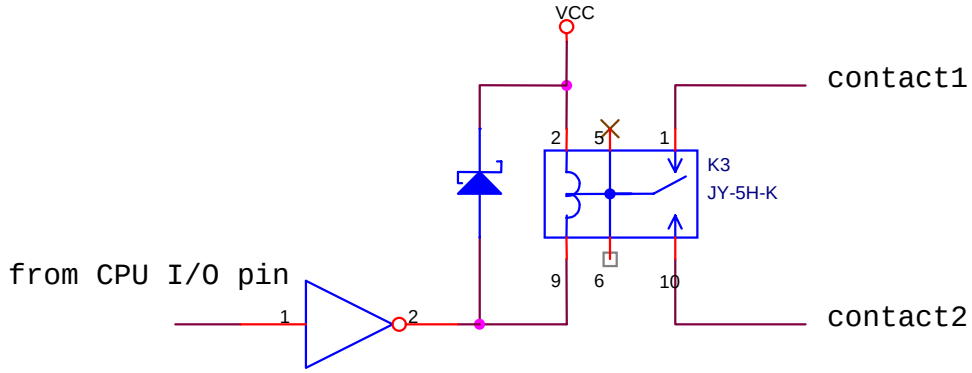


Figure 21. Relay DO

The relay output is a dry contact so there is no polarity of the contact 1 and 2. The relay used is a Takamisawa JY-5H-K type and is capable of load up to,

- 5A at 30VDC
- ?A at 125VAC
- ?A at 250VAC

23.LED

2 LEDs (green and red) are equipped to indicate working status and can be controlled by software.

24.Speaker & Ear-phone

A buzzer is equipped as the audio indicator. Its tone is software controllable whereas the volume is to be tuned via a variable resistor. Depending on application needs, an ear-phone can also be attached. The audio-jack has been intentionally designed to disable the buzzer while the ear-phone is connected. Usual ear-phone used in Walk-Man can be used with 520.

25.Wall-mount shelf

An optional metal case can be used if mounting on the wall is required.

26. Table stand

An optional table stand can be used if mounting on the table is required.